REMARKS

Summary of Claim Status

Claims 1-31 are pending in the present application after entry of the present amendment. Claims 1-17 and 22-31 are rejected for the reasons discussed below. Claims 18-21 are withdrawn.

Applicants request the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the following remarks.

Objection to the Specification

The specification is objected to because of certain informalities. Applicant has amended the specification as directed by the Examiner. Therefore, this objection is overcome.

Rejections Under 35 USC 102(e)

Claims 1-17 and 22-31 are rejected as being anticipated by "Bauer" (USPN 6,671,202). The Examiner therefore argues that Bauer teaches every element of every claim, either expressly or by implication. (MPEP 706.02(IV) provides the following summary of the relevant standard: "For anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.") Applicants respectfully traverse this rejection with regard to all claims.

Firstly, the rejection is traversed on the grounds that the claimed methods, media, and systems are clearly incompatible with the structures described by Bauer. In other words, the claimed methods cannot be practiced on Bauer's structures. Secondly, even if Bauer did in fact illustrate one or more structures on which the methods of the invention could be practiced (which Applicants do not concede), Bauer in fact neither teaches nor suggests applying the claimed methods to these or any other structures.

In Applicants' claimed methods, during implementation of a design in the PLD, a single node ("the node") is routed on two different paths through the same multiplexer ("the programmable routing multiplexer"), using two different data input terminals of the

multiplexer ("the first and second data input terminals"). A selection between the two input paths is controlled solely by a value stored in a single memory cell controlling the multiplexer ("the first memory cell"), and thus potentially subject to single event upset (SEU). However, because the selection is controlled solely by the contents of the one memory cell, such an SEU will merely change the selection from one of the paths to the other (e.g., from the first routing path to the second routing path, or *vice versa*), and they each provide the same input signal to the multiplexer on a different data input terminal. Thus, an SEU that incorrectly changes the select function of the multiplexer by changing the value stored in the select memory cell still leaves the multiplexer providing the correct output signal.

Bauer's Fig. 1 shows a structure in which there are no two input paths between which a selection is controlled solely by a value stored in a single memory cell. Each input path is controlled by a separate memory cell. Therefore, Fig. 1 does not illustrate a multiplexer in which "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer".

Bauer's Figs. 4 and 5 show structures in which at most one memory cell can have an enable value at any given time (see Bauer's abstract and Figs. 4 and 5). Thus, if a first pass gate is enabled by a value stored in a first memory cell, selecting a first path through the multiplexer, a second pass gate selecting a second path is necessarily disabled. If a single event upset (SEU) occurs in any of the disabling memory cells, the value stored in the memory cell does not change, and the associated paths remain disabled. If an SEU occurs in the enabling memory cell, the path associated with that memory cell becomes disabled. (Abstract.) Therefore, it is not possible for a single event upset to change a selection from one path to another path, but at most to change a selection of one path to no selected path. Therefore, these structures also fail to illustrate a multiplexer in which "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer". Therefore, not only do these structures render it impossible to perform the claimed identification:

> identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer (Claim 1)

but they also provide no motivation to route the node on two different routing paths as claimed:

> routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal; and
>
> routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal. (Claim 1)

because there is no advantage to doing so in Bauer's structures.

Therefore, Bauer neither teaches nor suggests a structure in which "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer". Since it is not possible to find two such input paths, the claimed methods cannot be practiced on such a structure.

Each of Claims 1, 8, 10, 12, 22, 28, and 30 specifies that "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer". Clearly, such a selection cannot be made using the structures of Bauer's Figs. 1, 4, and 5. Further, even if Bauer's figures did in fact illustrate a structure on which the methods of the invention could be practiced (which Applicants do not concede), Bauer in fact neither teaches nor suggests applying the claimed method steps. For example, Bauer neither teaches nor suggests routing the same node on both first and second routing paths through the routing multiplexer. Applicants are not claiming a multiplexer structure, but methods, media, and systems for implementing a design in a multiplexer structure, and Bauer clearly neither teaches nor suggests these methods, media, or systems.

Therefore, and for at least these reasons, Claims 1, 8, 10, 12, 22, 28, and 30 distinguish over Bauer. Claims 2-7, 9, 11, 13-17, 23-27, 29, and 31 also distinguish

over Bauer for at least the reasons of these claims, from which they respectively depend.

Applicants must also respectfully note that the rejection of Claims 7, 9, 11, 17, 27, 29, and 31 included in the Office Action is inadequate. These claims specify that the method/program/system further comprises evaluating the source and destination logic (or node) and determining that the source and destination logic (or node) do not form a portion of a triple modular redundancy (TMR) circuit. Bauer neither teaches nor suggests this feature of the claims. Therefore, Claims 7, 9, 11, 17, 27, 29, and 31 further distinguish over Bauer for at least this additional reason.

If the rejection of Claims 7, 9, 11, 17, 27, 29, and 31 is maintained, Applicants must respectfully request (as in Applicants' first Response) that this feature of the claims be addressed in its entirety.

Conclusion

No new matter has been introduced by any of the above amendments. All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,

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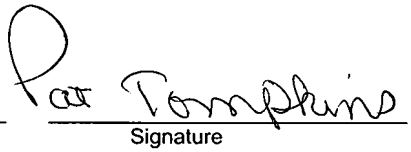

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